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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/440,595	11/15/1999	NAVEED MAJID	PHA-23843	3147

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/440,595	Majid et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Dec 20, 2001

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-7 is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-7 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2 and 10

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi et al (US Pat. 6130458) in view of Lauffer et al (IDS-paper #4, European Pat. 0471938A1) and the admitted prior art (APA- Japanese Pat. 6-169057A).

Regarding claims 1 and 5-7, Takagi et al disclose a multichip hybrid integrate circuit (IC)/module comprising:

-a power semiconductor chip and (200 in Fig. 12A and B) and a control semiconductor chip (100 in Fig. 12A and B) comprising silicon-on-insulator devices, and

- the power and control semiconductor chips being directly mounted on an electrically conductive substrate connected to ground potential (81 in Fig. 12B)

(Fig. 12A and B; Fig. 15; Col. 11, line 30-Col. 12, line 57).

Takagi et al fail to specify the control semiconductor chip comprising a bulk technology device and the electrically conductive substrate being a heat sink substrate.

Lauffer et al teach using a multichip module having a variety of chips such as high power, low power, memory, logic chip, etc. in the same package comprising a silicon chip on insulator/dielectric (115 in Fig. 4) and an integrated circuit (IC) chip (112 in Fig. 4) to improve heat dissipation and temperature distribution. Furthermore, chip 112 comprising a bulk/conventional technology device has no insulation layer between the device and substrate and is directly mounted on the electrically conductive heat sink/substrate made of copper (11 in Fig. 4; Col. 9, line 7) which is connected to a ground potential (Col. 12, line 32).

The APA and the cited reference (Hill- US Pat. 6028348, Fig, 3; Col. 2, line 66) teach using a multichip module with the chips mounted on a conventional metal/electrically conductive substrate which serves as a heat sink.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a control semiconductor chip comprising a bulk technology device and an electrically conductive heat sink substrate connected to ground potential to achieve improved heat dissipation, temperature distribution and to simplify processing using Lauffer et al and APA's chip/substrate structure in Takagi et al's multichip module.

Regarding claims 2-4, Takagi et al disclose the control semiconductor chip comprising CMOS or any other configurations comprising BICMOS, bipolar, n-MOS, etc. (Col. 13, line 64).

Response to Arguments

A. Applicant contends that Lauffer et al's structure is a complex structure and involves a plurality of insulating and conducting layers.

However, as explained above, Lauffer et al teaches using high and low power chips in the same package where a chip (112 in Fig. 4) comprising a bulk/conventional technology device without any insulation layer between the device and substrate is directly mounted on the electrically conductive heat sink/substrate while the other chips (113, 115, etc. in Fig. 4) have silicon on insulator/dielectric configuration. Therefore, Lauffer et al's configuration comprising the bulk/conventional technology is applied for the control chip in Takagi et al's module to improve the heat dissipation and temperature distribution.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

03-03-02

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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